



Embedded Xinu on the ARM 32F4 Discovery Board

By: Ethan Weber Department: Mathematics, Statistics, and Computer Science Mentor: Dr. Dennis Brylow



ARM		
er	Alias	
•	a1-a4	
•	v1-v8	
•	IP	
	SP	
	LR	
•	PC	
):	CPSR	

MIPS		
Register	Alias	
0:	zero	
1:	AT	
2-3:	v0-v1	
4-7:	a0-a1	
8-15:	t0-t7	
16-23:	s0-s7	
24-25:	t8-t9	
26-27:	k0-k1	
28:	s8	
29:	sp	
30:	s9	
31:	ra	